

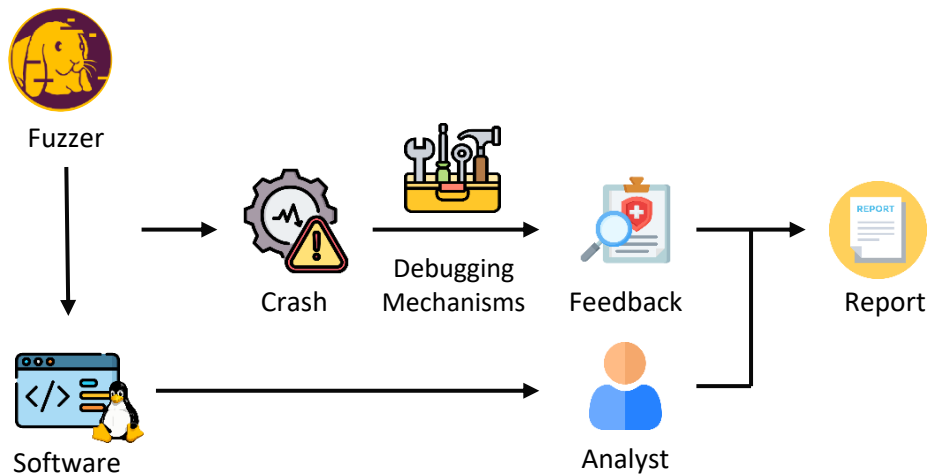
FirmRCA: Towards Post-Fuzzing Analysis on ARM Embedded Firmware with Efficient Event-based Fault Localization

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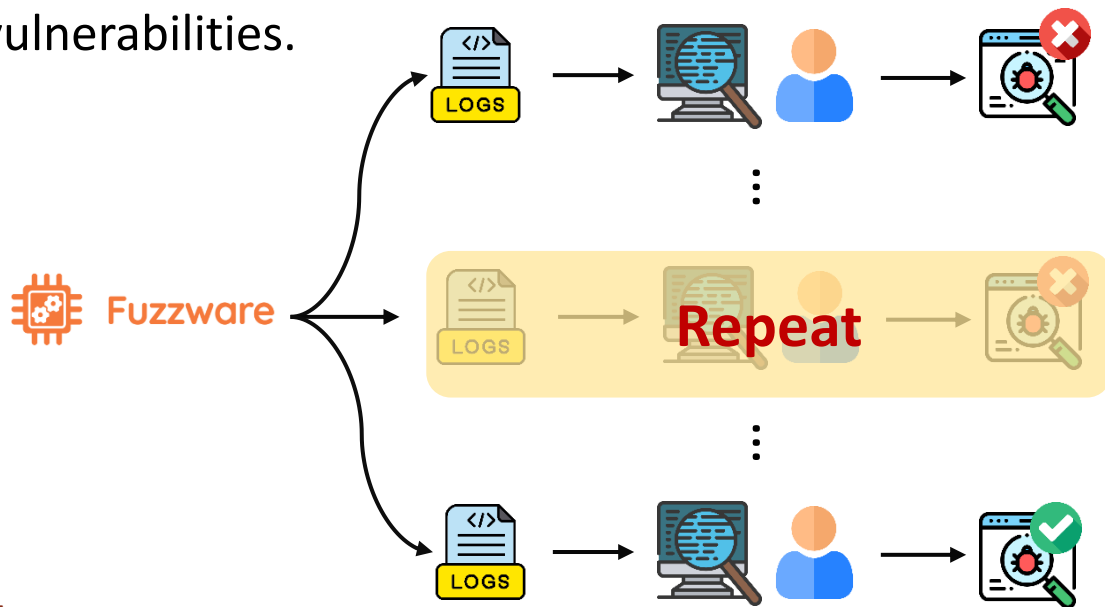


Motivation

- Firmware vulnerabilities threaten IoT devices.
- Fuzzing finds crashes, but fault localization (FL) is tedious and error-prone.

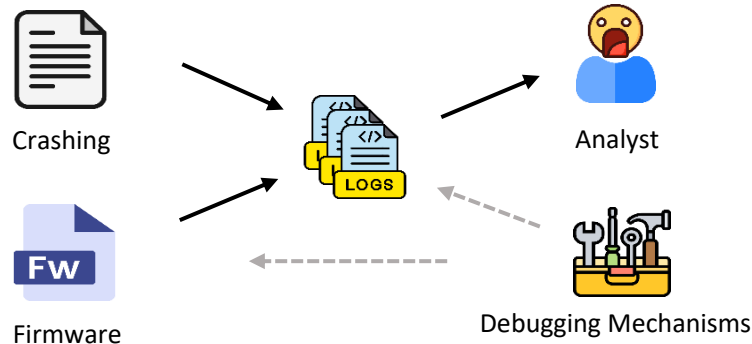
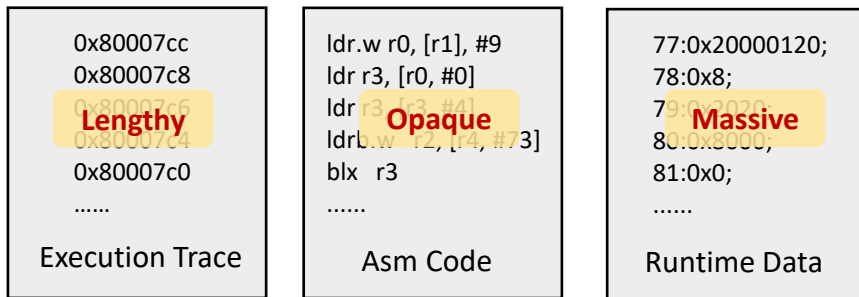


- After fuzzing, analysts face thousands of crashing test cases.
- Manual FL is inefficient, especially on stripped, raw binary firmware.
- Given limited analyst time, efficient FL is essential to prioritize and remediate critical vulnerabilities.

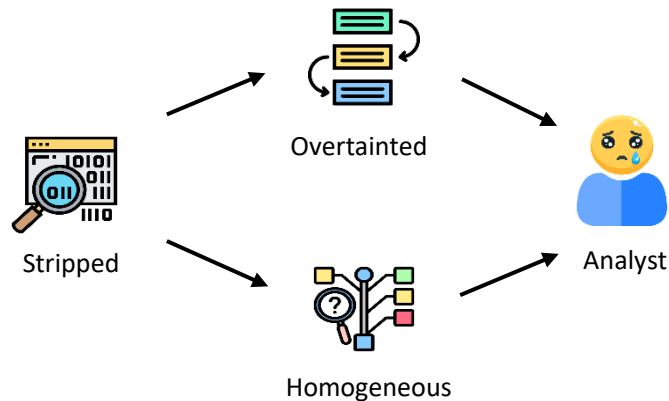
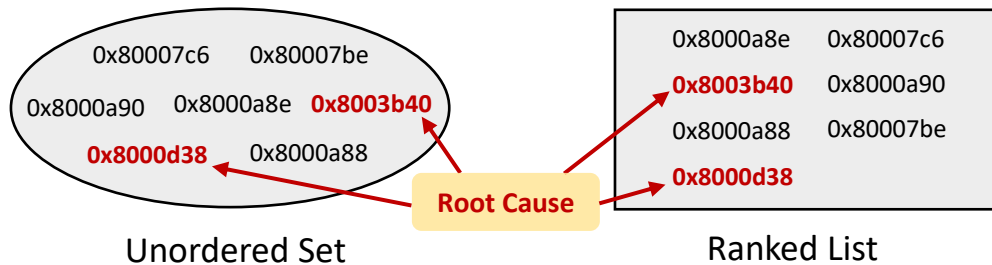


Challenges

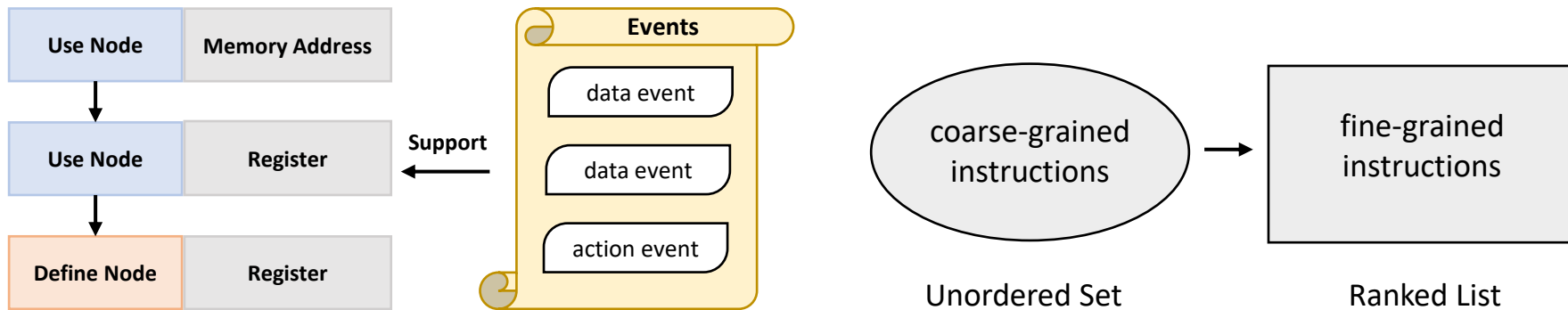
- **Challenge 1:** Inadequate debugging mechanisms.



- **Challenge 2:** Limited investigation guidance.

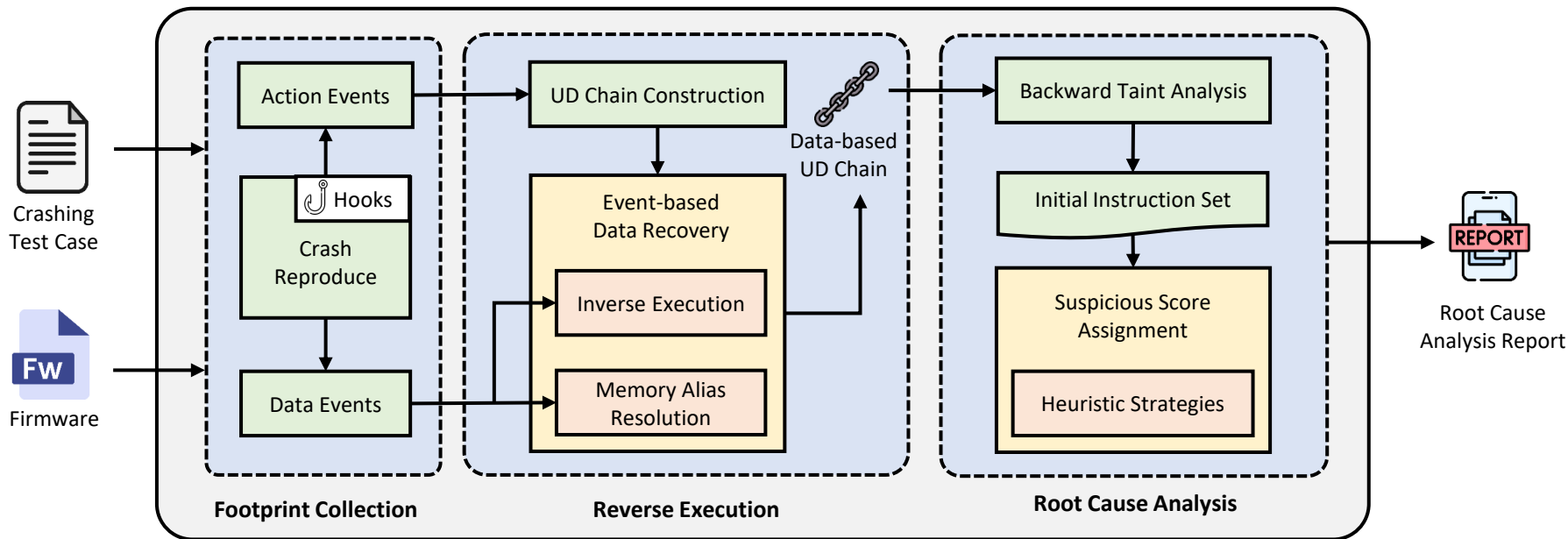


- **Inadequate debugging mechanisms:** reverse taint analysis from the crash site through a **data-based** use-define chain.
- **Limited investigation guidance:** tainted instructions are **not equally important**.



FirmRCA Overview

- Event-based data recovery enables precise memory resolution.
- Heuristic strategies prioritize root cause instructions.



- **Problem:** uncertain trace introduces huge time overhead and inaccuracy.
- **Solution:** event-based logging during crash reproduction.

```
net_6lo_uncompress:
0x406c74 PUSH.W {R3-R11, LR}
0x406c78 LDR  R6, [R0, #16]
0x406c7a LDR  R4, [R6, #8]  Crash!
0x406c7c LDRB R3, [R4, #0]
```

```
ieee802154_recv:
0x40d126 PUSH.W {R4-R8, LR}
...
0x40d1de BL    0x40d0a6    interprocedural
0x40d1e2 LDR  R0, [R4, #40]
0x40d1e4 CBZ  R0, 0x40d1f2 intraprocedural
0x40d1e6 LDRB R3, [R4, #44]
```

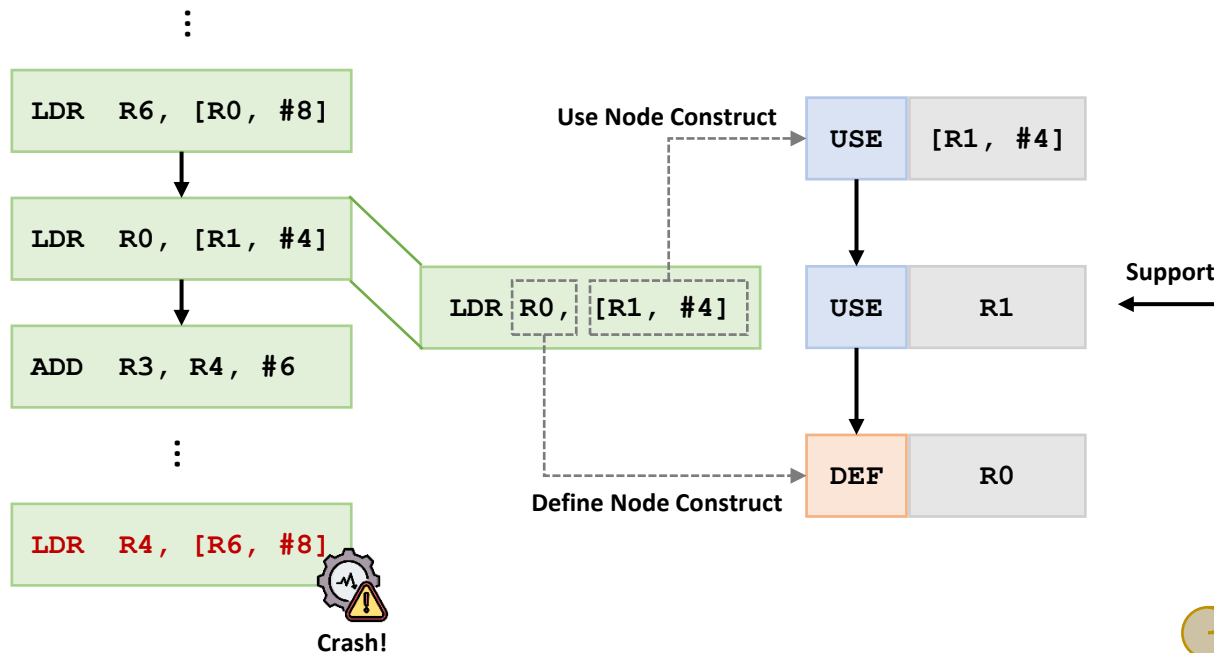
```
struct TraceEvent {
    union {
        instruction @0 :Instruction;
        access @1 :Access;
        dump @2 :Registers;
        crash @3 :Crash;
    }
}
```

```
struct Instruction {
    pc @0 :UInt32;
    lr @1 :UInt32;
}
```

```
struct Access {
    target @0 :AccessTarget;
    type @1 :UInt32;
    size @2 :UInt8;
    pc @3 :UInt32;
    address @4 :UInt32;
    value @5 :UInt32;
}
```



- Data-based use-define chain holds data flow.
- Inverse execution resolves unknown registers.



Events

[R1, #4] address
data event

[R1, #4] value
data event

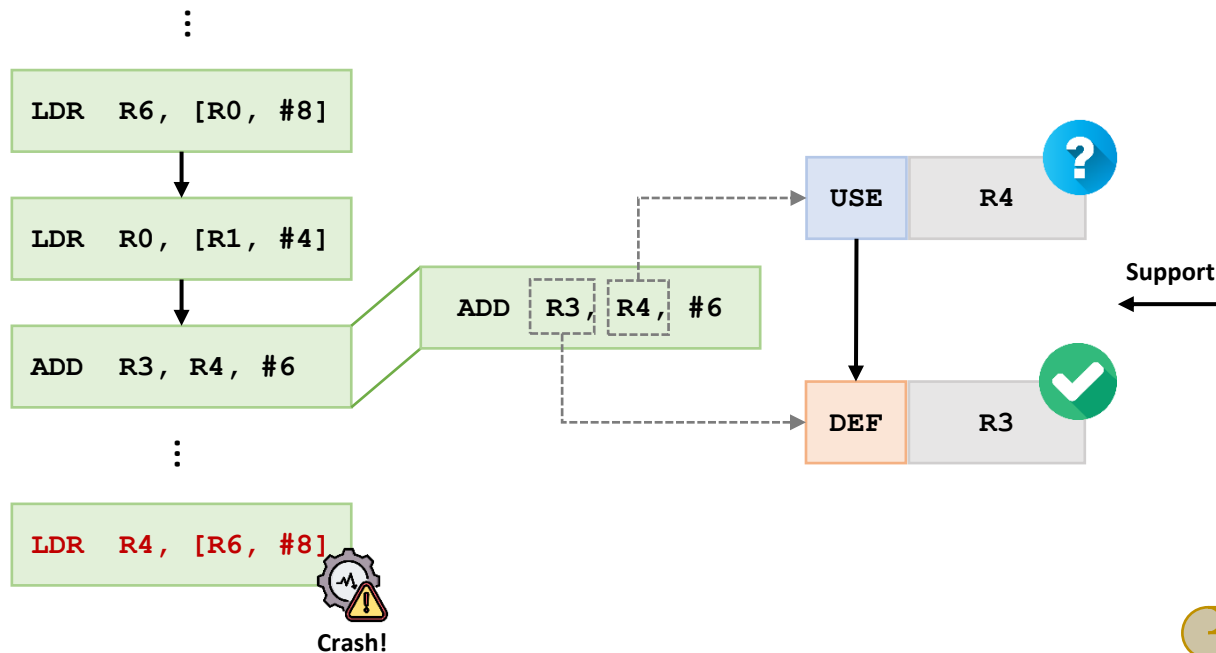
4 bytes
data event

R0 register
data event

PC value
action event

FirmRCA – Reverse Execution

- Data-based use-define chain holds data flow.
- Inverse execution resolves unknown registers.



Inverse handlers

ADD Rd, Rm

$Rd' = Rd + Rm$
 $Rd = Rd' - Rm$
 $Rm = Rd' - Rd$

ADD Rd, Rn, Rm

$Rd = Rn + Rm$
 $Rn = Rd - Rm$
 $Rm = Rd - Rn$

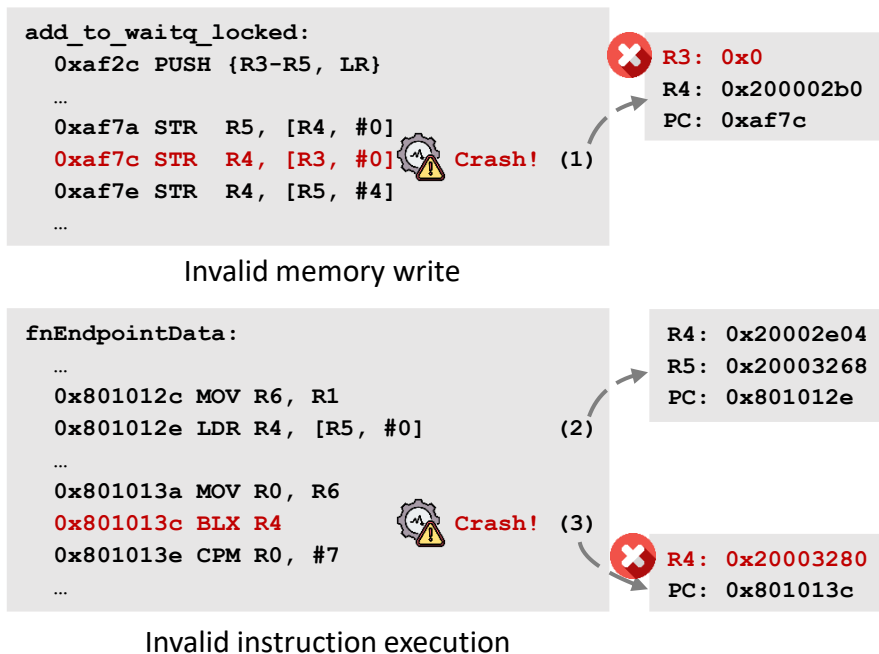
ADD Rd, Rn, #imm

$Rd = Rn + \text{imm}$
 $Rn = Rd - \text{imm}$

Support

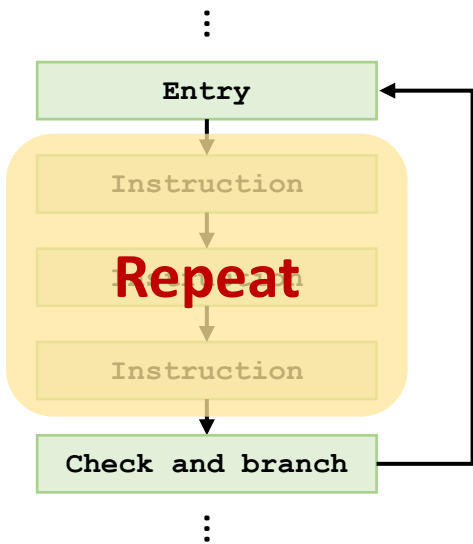
FirmRCA – Root Cause Analysis

- Two kinds of direct crash sites serve as the taint sink.
- Two kinds of heuristic ranking strategies for investigation guidance.

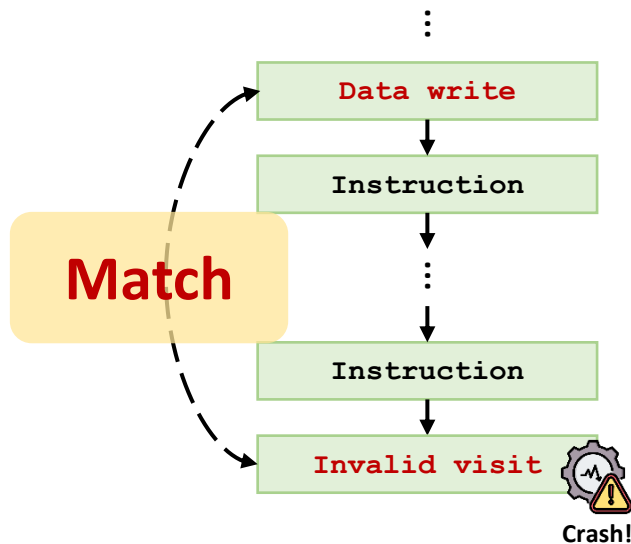


FirmRCA – Root Cause Analysis

- Two kinds of direct crash sites serve as the taint sink.
- Two kinds of heuristic ranking strategies for investigation guidance.



Redundant loop taint suppression



History write taint prioritization

Evaluation – Effectiveness

- FirmRCA identifies the root cause of 92.7% test cases in top 10 instructions.
- FirmRCA localizes deep root causes of 90.9% test cases.

ID	$\Delta\text{Root}(\%)$	# Traces	# Ins	Full			Half		
				P	P+	F	P	P+	F
C_1	2 (<0.1%)	52,080	11,869	$\emptyset$	$\times$	1	$\times$	$\times$	1
C_2	2 (<0.1%)	371,762	13,374	$\emptyset$	$\emptyset$	1	$\emptyset$	$\emptyset$	1
C_3	2 (<0.1%)	1,003,421	13,374	$\emptyset$	$\emptyset$	1	$\emptyset$	$\emptyset$	1
C_4	2 (<0.1%)	228,012	5,021	$\emptyset$	$\times$	1	$\emptyset$	$\times$	1
C_5	2 (<0.1%)	36,271	11,880	$\times$	$\times$	1	$\times$	$\times$	1
C_6	2 (<0.1%)	108,294	7,126	$\emptyset$	$\times$	1	$\emptyset$	$\times$	1
C_7	2 (<0.1%)	619,937	15,140	$\emptyset$	$\emptyset$	1	$\emptyset$	$\emptyset$	1
C_8	2 (<0.1%)	68,894	15,513	$\emptyset$	$\times$	1	$\times$	$\times$	1
C_9	2 (<0.1%)	524,897	11,931	$\emptyset$	$\emptyset$	1	$\emptyset$	$\emptyset$	1
C_{10}	20,203 (18.1%)	111,898	18,536	$\emptyset$	$\times$	2	$\times$	$\times$	2
C_{11}	78 (<0.1%)	168,542	17,165	$\emptyset$	1	1	1	1	1
C_{12}	120,472 (51.1%)	235,662	9,299	$\emptyset$	$\times$	<u>13</u>	$\times$	$\times$	8
C_{13}	2,176 (1.4%)	160,721	9,299	$\emptyset$	$\emptyset$	<u>21</u>	$\emptyset$	$\times$	19
C_{14}	8,155 (39.5%)	20,630	15,428	$\times$	$\times$	1	$\times$	$\times$	1
C_{15}	8,719 (73.0%)	11,943	17,165	$\times$	$\times$	1	$\times$	$\times$	$\times$
C_{16}	215,102 (98.7%)	217,900	17,165	$\emptyset$	$\times$	10	$\emptyset$	$\times$	$\times$
C_{17}	5,183 (3.0%)	173,913	17,165	$\emptyset$	8	1	$\times$	8	1
C_{18}	2,759 (1.6%)	169,666	17,165	$\emptyset$	$\times$	1	$\times$	$\times$	1
C_{19}	5,161 (72.2%)	7,151	9,299	$\times$	$\times$	1	$\times$	$\times$	$\times$
C_{20}	306 (<0.1%)	523,873	14,325	$\emptyset$	$\times$	1	$\times$	$\times$	1
C_{21}	2,013 (1.3%)	150,995	19,706	$\emptyset$	$\times$	2	$\times$	$\times$	2

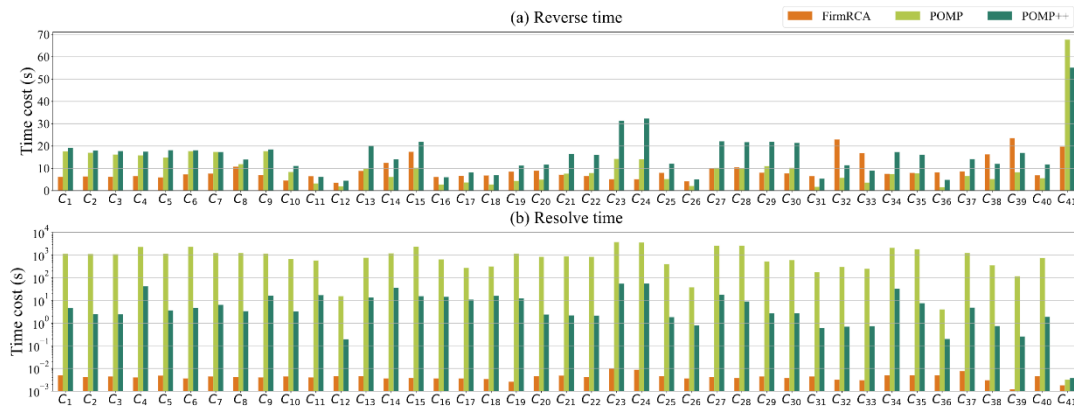
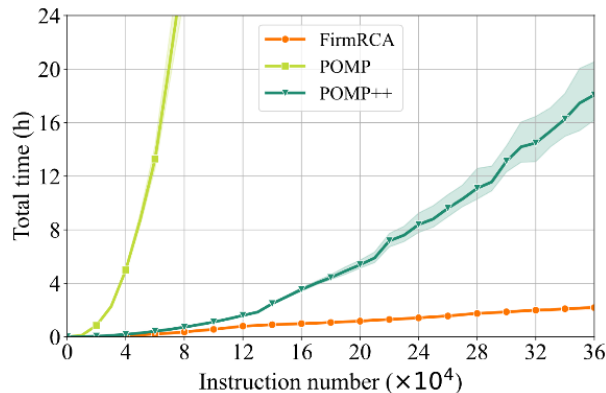
ID	$\Delta\text{Root}(\%)$	# Traces	# Ins	Full			Half		
				P	P+	F	P	P+	F
C_{22}	401 (0.2%)	238,470	13,954	$\emptyset$	$\times$	2	$\emptyset$	$\times$	2
C_{23}	53 (<0.1%)	89,136	32,546	$\emptyset$	$\times$	1	$\emptyset$	$\times$	1
C_{24}	53 (0.1%)	52,909	32,546	$\emptyset$	$\times$	1	$\emptyset$	$\times$	1
C_{25}	1,789 (0.4%)	434,172	13,954	$\emptyset$	1	2	$\emptyset$	1	2
C_{26}	88,746 (45.2%)	196,313	29,993	$\emptyset$	3	1	3	3	1
C_{27}	27,411 (58.2%)	47,065	15,529	3	3	3	3	3	4
C_{28}	28,771 (58.9%)	48,880	15,529	2	2	2	2	2	3
C_{29}	55,768 (66.4%)	84,028	23,706	$\emptyset$	$\times$	1	$\times$	$\times$	$\times$
C_{30}	59,717 (63.3%)	94,362	23,706	$\emptyset$	$\times$	1	$\times$	$\times$	$\times$
C_{31}	402 (<0.1%)	514,772	14,325	$\times$	$\times$	1	$\times$	$\times$	1
C_{32}	86,956 (8.7%)	994,960	27,664	$\emptyset$	$\emptyset$	<u>$\times$</u>	$\emptyset$	$\emptyset$	$\times$
C_{33}	100,512 (48.2%)	208,669	18,464	$\emptyset$	2	2	$\emptyset$	2	3
C_{34}	21 (<0.1%)	160,958	18,475	$\emptyset$	$\times$	1	$\emptyset$	$\times$	1
C_{35}	337 (<0.1%)	1,960,419	26,165	$\emptyset$	$\emptyset$	1	$\emptyset$	$\emptyset$	1
C_{36}	274,858 (27.1%)	1,016,078	26,167	$\emptyset$	$\emptyset$	1	$\emptyset$	$\emptyset$	$\times$
C_{37}	1,458,974 (99.0%)	1,474,404	18,202	$\emptyset$	$\emptyset$	1	$\emptyset$	$\emptyset$	$\times$
C_{38}	44,256 (3.4%)	1,300,470	25,887	$\emptyset$	$\emptyset$	1	$\emptyset$	$\emptyset$	1
C_{39}	42,177 (53.6%)	78,624	15,605	$\emptyset$	$\times$	1	$\times$	$\times$	1
C_{40}	891 (1.7%)	52,173	11,952	4	4	5	4	4	5
C_{41}	594,471 (95.1%)	625,021	12,258	$\emptyset$	$\emptyset$	1	$\emptyset$	$\times$	$\times$

ΔRoot denotes the distance between the root cause and crash site; $\emptyset$ indicates the analysis timed out; $\times$ indicates the root cause is not found
Failures in the FirmRCA analysis of full instructions are underlined; ID is highlighted in **GRAY** if its ΔRoot is larger than 50%



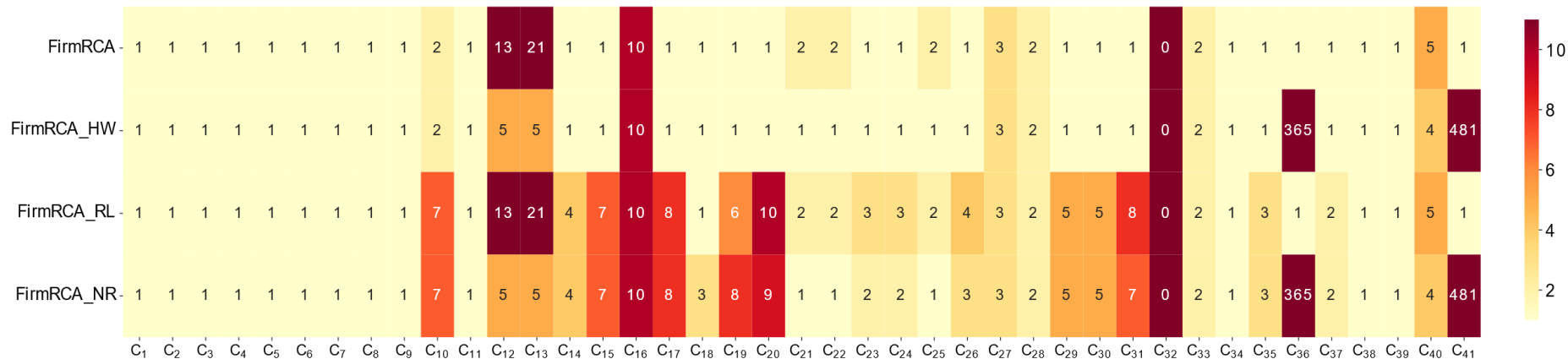
Evaluation – Efficiency

- FirmRCA shows a modest overall time cost as the analysis depth increases.
- The efficient memory alias resolution is a key contributor.



Evaluation – Ranking Strategies

- All four prototypes demonstrate high success rates.
- *Firm_RL* helps level up the rank to the top 1.
- *Firm_HW* enhances the ranking results in 36.6% of the test cases.



FirmRCA_NR: no ranking strategies enabled; *FirmRCA_RL*: the redundant loop taint suppression strategy enabled

FirmRCA_HW: the history write prioritization strategy enabled; *FirmRCA*: both ranking strategies enabled



FirmRCA: Towards Post-Fuzzing Analysis on ARM Embedded Firmware with Efficient Event-based Fault Localization

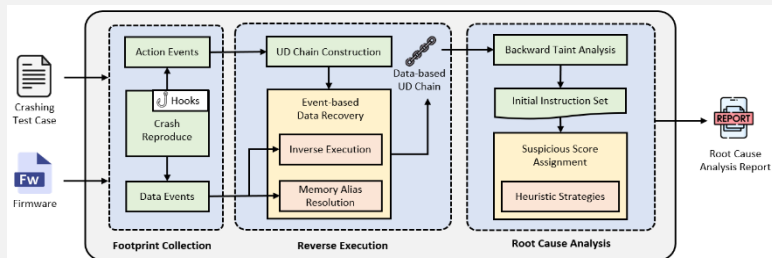
Challenges

Challenge 1: Inadequate debugging mechanisms.

Challenge 2: Limited investigation guidance.

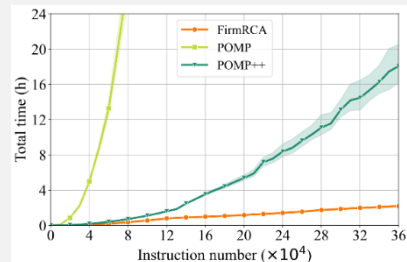
FirmRCA Framework

An efficient event-based fault localization work.



Effectiveness and Efficiency

ID	$\Delta\text{Reoc}(\%)$	# Traces	# Ins	Full			Half		
				P	P ¹	F	P	P ¹	F
C ₁	2 (<0.1%)	52,080	11,869	0	X	1	X	X	1
C ₂	2 (<0.1%)	371,762	13,374	0	0	1	0	0	1
C ₃	2 (<0.1%)	1,003,421	13,374	0	0	1	0	0	1
C ₄	2 (<0.1%)	228,012	5,021	0	X	1	0	X	1
C ₅	2 (<0.1%)	36,271	11,880	X	X	1	X	X	1
C ₆	2 (<0.1%)	108,294	7,126	0	X	1	0	X	1
C ₇	2 (<0.1%)	610,937	15,140	0	0	1	0	0	1
C ₈	2 (<0.1%)	68,894	15,513	0	X	1	X	X	1
C ₉	2 (<0.1%)	574,897	11,911	0	0	1	0	0	1
C ₁₀	20,203 (18.1%)	111,898	18,536	0	X	2	X	X	2
C ₁₁	78 (<0.1%)	168,512	17,165	0	1	1	1	1	1
C ₁₂	120,472 (51.1%)	235,662	9,289	0	X	13	X	X	8
C ₁₃	2,176 (1.4%)	160,721	9,289	0	0	21	0	X	19
C ₁₄	8,155 (39.5%)	20,630	15,428	X	X	1	X	X	1
C ₁₅	8,719 (73.0%)	11,943	17,165	X	X	1	X	X	X
C ₁₆	215,102 (98.7%)	217,980	17,165	0	X	10	0	X	X
C ₁₇	5,183 (3.0%)	173,913	17,165	0	8	1	X	8	1
C ₁₈	2,739 (1.6%)	169,666	17,165	0	X	1	X	X	1
C ₁₉	5,161 (72.2%)	7,151	9,289	X	X	1	X	X	X
C ₂₀	306 (<0.1%)	523,873	14,325	0	X	1	X	X	1
C ₂₁	2,013 (1.3%)	150,995	19,706	0	X	2	X	X	2



Paper



Code



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